Amendments to the Claims

The listing of claims below will replace all prior versions and listings of claims in the application.

1-7. (Cancelled)

8. (Currently Amended) Simulation system for simulation of an electronic circuit, the circuit being representable by a network of logical elements, ~~the circuit~~ comprising:

a first asynchronous clock domain; [[and]]

a second asynchronous clock domain, coupled to the first asynchronous clock domain, including one or more jitter elements, wherein at least one of the one or more jitter elements ~~are additionally~~ is insertable in the second asynchronous clock domain at ~~predetermined portions of~~ a circuit ~~boundaries~~ boundary between the first asynchronous clock domain and the second asynchronous clock domain. ~~domain, the jitter elements being representable as logical elements, the values of which are randomly set, wherein at least one of the jitter elements is configured to jitter data from the first asynchronous clock domain.~~

9. (Cancelled)

10. (Currently Amended) The system of claim 8, wherein the at least one of the one or more jitter elements comprise one or more delay elements for introducing predetermined timing delays which are randomly exercised.

11. (Currently Amended) The system of claim 8, wherein the at least one of the one or more jitter elements comprise x generator elements for introducing predetermined signal values which are randomly generated.

12. (Currently Amended) The system of claim 8, wherein the at least one of the one or more jitter elements are interactively inserted by a user.

13. (Currently Amended) The system of claim 8, wherein the at least one of the one or more jitter elements are automatically inserted using predetermined modules.

14-15. (Cancelled)

16. (New) The system of claim 8, wherein the one or more jitter elements are representable as logical elements, the values of which are randomly set.

17. (New) The system of claim 8, wherein at least one of the one or more jitter elements is configured to jitter data from the first asynchronous clock domain.

18. (New) An electronic circuit representable by a network of logical elements, comprising:

a first asynchronous clock domain;

a second asynchronous clock domain, coupled to the first asynchronous clock domain, including one or more jitter elements, wherein at least one of the one or more jitter elements is insertable in the second asynchronous clock domain at a circuit boundary between the first asynchronous clock domain and the second asynchronous clock domain.

19. (New) The circuit of claim 18, wherein the at least one of the one or more jitter elements comprise one or more delay elements for introducing predetermined timing delays which are randomly exercised.

20. (New) The circuit of claim 18, wherein the at least one of the one or more jitter elements comprise x generator elements for introducing predetermined signal values which are randomly generated.

21. (New) The circuit of claim 18, wherein the at least one of the one or more jitter elements are interactively inserted by a user.

22. (New) The circuit of claim 18, wherein the at least one of the one or more jitter elements are automatically inserted using predetermined modules.